

Notice of References Cited		Application/Control No.	Applicant(s)/Patent Under Reexamination	
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Examiner		Art Unit		Page 1 of 1
Kandasamy Thangavelu		2123		

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	B	US-5,910,897	06-1999	Dangelo et al.	364/488
	C	US-			
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

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NON-PATENT DOCUMENTS

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	U	Bogliolo et al., "Reliability evaluation of combinational logic circuits by symbolic simulation", IEEE 1995
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.